WHAT IS CLAIMED IS:

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1. A semiconductor device comprising: a bleeder resistance circuit having a plurality of thin film resistors are on a first conductor through a first insulating film and the first conductor under the thin film resistors and the thin film resistors are made to have substantially the same potential.

2. A semiconductor device according to claim 1, wherein a second insulating film is formed on the thin film resistors, a second conductor is formed on the second insulating film in a position over the thin film resistors, and the thin film resistors and the second conductor are made to have substantially the same potential.

3. A semiconductor device according to claim 1, wherein the first conductor corresponding to each of the plurality of thin film resistors has substantially the same potential as each of the plurality of thin film resistors.

4. A semiconductor device according to claim 2, wherein the second conductor corresponding to each of the plurality of thin film resistors has substantially the same potential as each of the plurality of thin film resistors.

5. A semiconductor device according to claim 1, wherein the thin film resistors are polysilicon.

6. A semiconductor device according to claim 2, wherein

the thin film resistors are polysilicon.

7. A semiconductor device according to claim 5 or 6, wherein an impurity introduced into the thin film resistors is of a P-type.

8. A semiconductor device according to claim 7, wherein the P-type impurity introduced into the thin film resistors is BF_2.

9. A semiconductor device according to claim 7, wherein the P-type impurity introduced into the thin film resistors is boron.

10. A semiconductor device according to claim 5 or 6, wherein a film thickness of the thin film resistors is several tens to 2000 angstroms.

11. A semiconductor device according to claim 5 or 6, wherein a film thickness of the thin film resistors is several tens to 1000 angstroms.

12. A semiconductor device according to claim 5 or 6, wherein the first conductor is made from a well region formed in a silicon substrate.

13. A semiconductor device according to claim 5 or 6, wherein the first conductor is made of polysilicon.

14. A semiconductor device according to claim 6, wherein the second conductor is made of polysilicon.

15. A semiconductor device according to claim 6, wherein

the second conductor is made of aluminum.

16. A semiconductor device according to claim 6, wherein the second conductor is made from a lamination film of a barrier metal and a silicide film.

17. A semiconductor device according to claim 6, wherein the first conductor is made of a material constituting a gate electrode of an MOS type transistor which is formed together with the plurality of thin film resistors on a single chip.

18. A semiconductor device according to claim 5 or 6, wherein the potential of each of the plurality of thin film resistors and the potential of the first conductor corresponding to each of the thin film resistors are fixed by a metal wiring material through a common contact hole.

19. A semiconductor device according to claims 5 and 6, wherein, in the semiconductor device which has a bleeder resistance circuit using the plurality of thin film resistors and at least one MOS type transistor, a film thickness of the thin film resistors of the bleeder resistance circuit is formed thinner than that of a gate electrode of the MOS type transistor.

20. A semiconductor device according to claim 19, wherein the film thickness of the thin film resistors is several tens to 1000 angstroms.

21. A semiconductor device according to claim 19, wherein

an impurity introduced into the thin film resistors is of a P-type.

22. A semiconductor device according to claim 21, wherein the P-type impurity introduced into the thin film resistors is BF_2.

23. A semiconductor device according to claim 21, wherein the P-type impurity introduced into the thin film resistors is boron.

24. A semiconductor device according to claim 19, wherein a temperature dependency of a resistance value of the thin film resistors is -4000 ppm/°C or less.

25. A semiconductor device according to claim 5 or 6, wherein, in the semiconductor device having the thin film resistors, the thin film resistors are made from a low resistance region which is connected with a metal wiring and has a high impurity concentration and a high resistance region, and a film thickness of the high resistance region is smaller than that of the low resistance region.

26. A semiconductor device according to claim 25, wherein the film thickness of the high resistance region is several tens to 1000 angstroms and the film thickness of the low resistance region is 2000 to 10000 angstroms.

27. A semiconductor device according to claim 25, wherein the low resistance region and the high resistance region of

the thin film resistors are formed on the same flat surface.

28. A semiconductor device according to claim 25, wherein the upper surface of the low resistance region and the high resistance region of the thin film resistors forms the same flat surface.

29. A semiconductor device according to claim 5 or 6, wherein the first insulating film and the second insulating film are made of a silicon oxide film.

30. A semiconductor device according to claim 5 or 6, wherein at least one of the first insulating film and the second insulating film are made of a multilayer film including a silicon nitride film.

31. A semiconductor device according to claim 5 or 6, wherein a resistance value of the entire bleeder resistance circuit using the plurality of thin film resistors is 1 megaohm to 100 megaohms.

32. A method of manufacturing a semiconductor device, comprising the steps of:

preparing a silicon substrate to form a plurality of selectively separated and independent well regions by an ion implantation method;

selectively forming a field oxide film by the LOCOS method in the surface of the silicon substrate;

forming a gate oxide film, performing a channel dope for

a predetermined threshold control, depositing a polysilicon layer by a CVD method, and selectively introducing an impurity into the polysilicon layer by an ion implantation method so as to obtain a predetermined sheet resistance value;

after selectively introducing an impurity such as phosphorus with a high concentration into the polysilicon layer such that a predetermined region of the polysilicon layer has a low resistance, processing the polysilicon layer by etching into a predetermined shape such that a gate electrode with a low resistance and a plurality of polysilicon resistors each having a high resistance region are matched with the well regions, and locating the gate electrode and the polysilicon resistors;

introducing an N-type impurity such as phosphorus by an ion implantation method to form a source region and a drain region of an N-type transistor;

introducing a P-type impurity by an ion implantation method to form a source region and a drain region of a P-type transistor and a low resistance region of each of the polysilicon resistors;

depositing an intermediate insulating film, and subsequently forming a contact hole;

depositing an aluminum layer as a wiring by a sputtering method, and then patterning the aluminum layer such that the

aluminum layer connected with the low resistance region in one end of each of the polysilicon resistors and each of the well regions is located on each of the polysilicon resistors; and

forming a protective film, and removing a portion of the protective film to provide a region of a bonding pad and the like.

33. A method of manufacturing a semiconductor device, comprising the steps of:

preparing a silicon substrate to form a plurality of selectively separated and independent well regions by an ion implantation method, and selectively forming a field oxide film by the LOCOS method;

after forming a gate oxide film, performing a channel dope for a predetermined threshold control, depositing a first polysilicon layer by a CVD method, and introducing an impurity such as phosphorus with a high concentration into the first polysilicon layer such that the first polysilicon layer has a low resistance;

processing the first polysilicon layer by etching into a predetermined shape to form a gate electrode with a low resistance and a plurality of low resistance polysilicon layers;

forming a first insulating film by a thermal oxidation method or a CVD method;

depositing a second polysilicon layer with a film thickness thinner than that of the first polysilicon layer, and introducing an impurity into the second polysilicon layer by an ion implantation method so as to obtain a predetermined sheet resistance value;

patterning the second polysilicon layer such that a plurality of polysilicon resistors using the second polysilicon layer are formed on the independent low resistance polysilicon layers through the first insulating film;

introducing an N-type impurity such as phosphorus by an ion implantation method to form a source region and a drain region of an N-type transistor;

introducing a P-type impurity by an ion implantation method to form a source region and a drain region of a P-type transistor together with a low resistance region in a portion of each of the polysilicon resistors;

depositing an intermediate insulating film, and forming a common contact hole such that the low resistance region of each of the polysilicon resistors and each of the low resistance polysilicon layers can be connected with each other through the common contact hole;

depositing an aluminum layer as a wiring by a sputtering method, and patterning the aluminum layer such that the aluminum layer for connecting, the low resistance region in

one end of each of the polysilicon resistors, with each of the low resistance polysilicon layers located under each of the polysilicon resistors through the first insulating film, through the common contact hole, is located on each of the polysilicon resistors; and

forming a protective film, and removing a portion of the protective film to provide a region of a bonding pad and the like.

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